THIN FILM TRANSISTOR ARRAY SUBSTRATE AND MANUFACTURING METHOD THEREOF

DESCRIPTION

BACKGROUND OF THE INVENTION

[Para 1] Field of the Invention

[Para 2] The present invention relates to a display panel and manufacturing method thereof. More particularly, the present invention relates to a thin film transistor array substrate and manufacturing method thereof.

[Para 3] Description of the Related Art

[Para 4] With the increase in computing power and the rapid development of Internet and multimedia technologies, most image data are transmitted in digital format rather than analogue format. To match the life style of modern people, video or image devices have been developed to be small and compact. In the past, conventional cathode ray tubes (CRT) used to be the dominant display devices because their high display quality and a low cost features. However, with the recent campaign for protecting the environmental, its bulkiness, high power consumption and high radiation makes it less desirable paving a way to develop display devices that are small, compact and energy-saving and low radiations.

[Para 5] In recent years, with great advance in the technique of fabricating electrical-optical and semiconductor devices, flat panel displays, such as a liquid crystal displays (LCD), have developed. Due to the

advantageous features provided by the LCD, namely, a low operating voltage, free of harmful radiation, light weight and small and compact size, liquid crystal displays (LCD) have gradually replaced the conventional CRT and has become the mainstream display products.

[Para 6] Fig. 1 is a schematic cross-sectional view of a conventional liquid crystal display module. To simplify the drawing, only the components necessary for the explanation are shown in Fig. 1. The liquid crystal display module shown in Fig. 1 comprises a thin film transistor array substrate 110, a color filter substrate 120 including a black matrix layer 122 thereon, a seal 130, a liquid crystal layer 140, polarizing plates 152, 154 and an external frame 160. The seal 130 is disposed between the color filter substrate 120 and the thin film transistor array substrate 110 for sealing the color filter substrate 120 and the thin film transistor array substrate 110. The liquid crystal layer 140 is disposed within the space bounded by the color filter substrate 120, the thin film transistor array substrate 110 and the seal 130. Furthermore, the polarizing plates 152, 154 are disposed on the exterior surface of the thin film transistor array substrate 110 and the color filter substrate 120 respectively. The outer frame 160 is disposed on the polarizing plate 152. In addition, the thin film transistor array substrate 110 can be divided into a pixel region 110a and a peripheral region 110b. The peripheral region 110b has a plurality of lead lines 112 therein for connecting pixels in the pixel region 110a and peripheral circuits in the peripheral region 110b.

[Para 7] The conventional method of filling the liquid crystal layer 140 includes forming a sealed space between the thin film transistor array substrate 110 and the color filter substrate 120 using the seal 130. Thereafter, liquid crystal is slowly injected into the aforementioned sealed space through the capillary effect under the atmospheric pressure. Because the injection process is rather slow, it is unsuitable for fabricating large size liquid crystal display panel. To increase the speed of the fabrication process, a liquid crystal drop filling (ODF) method for fabricating LCD panel has been developed. In the ODF method, the seal 130 is formed on the thin film transistor array substrate 110 or the color filter substrate 120. Liquid crystal

is dropped into an area enclosed by the seal 130. Thereafter, the thin film transistor array substrate 110 and the color filter substrate 120 are sealed together. Finally, the seal 130 is irradiated with ultraviolet light to cure the seal 130 and bond the thin film transistor array substrate 110 and the color filter substrate 120 together.

[Para 8] To prevent the incompletely irradiated seal material from contaminating the liquid crystal 140, the black matrix layer 122 on the color filter substrate 100 is shrunk towards the center of the panel by a short distance. However, with the black matrix layer 122 slightly contracted, a light-leaking area 170 is formed between the black matrix layer 122 and the seal 130. In addition, there is no shade in the area between the lead lines 112 within the peripheral region 110b. Hence, light 180 emitted from the back light module may pass through the areas between the lead lines 112 and produce a vertical or slant light beam at the junction between the outer frame 160 and the thin film transistor array substrate 110.

SUMMARY OF THE INVENTION

[Para 9] Accordingly, the present invention is directed to a thin film transistor array substrate and a fabricating method thereof capable of resolving the problem of light leakage from a peripheral region.

[Para 10] The present invention provides a thin film transistor array substrate is provided. The thin film transistor array substrate comprises a pixel region and a peripheral region surrounding the pixel region. The thin film transistor array substrate comprises a transparent substrate, a thin film transistor array, a plurality of first lead lines, a plurality of second lead lines and a first shielding layer. The thin film transistor array is disposed on the transparent substrate within the pixel region. The thin film transistor array comprises at least a first conductive layer and a second conductive layer. The first lead lines are disposed over the transparent substrate within the

peripheral region. The first lead lines and the first conductive layer are the same film layer. Similarly, the second lead lines are disposed over the transparent substrate within the peripheral region. The second lead lines and the second conductive layer are the same film layer. The first shielding layer is disposed over the transparent substrate within the peripheral region, and the first shielding layer and the second conductive layer are the same film layer. Especially, the first shielding layer is disposed covering the gaps between neighboring first lead lines.

[Para 11] The present invention is also directed to a method of fabricating a thin film transistor array substrate. A transparent substrate having a pixel region and a peripheral region is provided. A patterned gate layer is formed in the pixel region, and a plurality of first lead lines and a plurality of first bonding pads connected to the first lead lines are formed in the peripheral region simultaneously. An insulating layer is formed over the transparent substrate to cover the gate layer and the first lead lines. A patterned channel layer is formed over the insulating layer above the gate layer. A patterned source/drain layer is formed over the channel layer, and a plurality of second lead lines and a plurality of second bonding pads connected to the lead lines are formed in the peripheral region. Particularly, the process of forming the source/drain layer further includes forming a first shielding layer covering the gaps between neighboring first lead lines.

[Para 12] The present invention is also directed to an alternative method of fabricating a thin film transistor array substrate. First, a transparent substrate having a pixel region and a peripheral region is provided. Thereafter, a patterned gate layer is formed in the pixel region and a plurality of first lead lines and a plurality of first bonding pads connected to various first lead lines are formed in the peripheral region. An insulating layer is formed over the transparent substrate to cover the gate layer and the first lead lines. A patterned channel layer is formed over the insulating layer above the gate layer. A patterned source/drain layer is formed over the channel layer and a plurality of second lead lines and a plurality of second bonding pads connected to various lead lines are formed in the peripheral region.

Particularly, the process of forming the gate layer further includes forming a shielding layer in a location underneath the subsequently formed gaps between neighboring second lead lines.

[Para 13] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 14] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[Para 15] Fig. 1 is a schematic cross-sectional view of a conventional liquid crystal display module.

[Para 16] Fig. 2 is a top view of a thin film transistor array according to an embodiment of the present invention.

[Para 17] Fig. 3 is a cross-sectional view showing a local section of a thin film transistor array according to an embodiment of the present invention.

[Para 18] Fig. 4 is a magnified cross-sectional view showing a structural layout of gate lines in the peripheral region according to an embodiment of the present invention.

[Para 19] Fig. 5 is a magnified cross-sectional view showing a structural layout of source lines in the peripheral region according to an embodiment of the present invention.

[Para 20] Figs. 6 and 7 are top views showing first bonding pads and second bonding pads according to another embodiment of the present invention.

[Para 21] Figs. 8A through 8E are schematic cross-sectional views showing the steps of fabricating a thin film transistor array substrate according to an embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[Para 22] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[Para 23] Fig. 2 is a top view of a thin film transistor array according to an embodiment of the present invention. Fig. 3 is a cross-sectional view showing a local section of a thin film transistor array according to an embodiment of the present invention. As shown in Fig. 2, the thin film transistor array substrate 210 includes a pixel region 210a and a peripheral region 210b surrounding the pixel region 210a. A thin film transistor array 212 comprising a plurality of thin film transistors and a plurality of pixel electrodes (not shown) are disposed on a transparent substrate 202 within the pixel region 210a. A plurality of lead lines such as gate lines 232 or source lines 234 linking with the thin film transistor array is disposed on the transparent substrate 202 within the peripheral region 210b. In addition, one end of each gate line 232 and the source line 234 are connected to a first bonding pad 232a and a second bonding pad 234a respectively for connecting to external circuits. As shown in Fig. 3, the thin film transistor array 212 comprises a gate layer 214, an insulating layer 216, a channel layer 218, a source/drain layer 220 and a passivation layer 222, for example. The gate lines 232 and the gate layer 214 are comprised of the same film layer.

[Para 24] As shown in Fig. 3, to reduce light leaking from the gaps between the gate lines 232 in the peripheral region 210b, a patterned first shielding layer 242 is formed over the gate lines 232 in the peripheral region 210b. The first shielding layer 242 at least covers the gaps between neighboring gate lines 232. Furthermore, the first shielding layer 242 and the source/drain layer 220 may be fabricated together in the same process. Fig. 4 is a magnified cross-sectional view showing the structural layout of the gate line 232 and the first shielding layer 242 according to an embodiment of the present invention. Similarly, the gaps between the source lines 234 in the peripheral region 210b may be covered with another shielding layer as shown in Fig. 5. Fig. 5 is a magnified cross-sectional view showing a structural layout of the source line 234 in the peripheral region 210b according to an embodiment of the present invention. As shown in Fig. 5, a patterned second shielding layer 244 is formed under the source line 234 in a location between the gaps of neighboring source lines 234. The second shielding layer 244 and the gate layer 214 may be fabricated together in the same process, for example. In an embodiment of the present invention, at least one of the first shielding layer 242 and the second shielding layer 244 are formed over the substrate 202. In another embodiment, both the first shielding layer 242 and the second shielding layer 244 are formed over the substrate 202.

[Para 25] The thin film transistor array substrate 210, according to an embodiment of the present invention, utilizes the first shielding layer 242 and the second shielding layer 244 to cover the gaps between neighboring gate lines 232 or neighboring source lines 234. The first shielding layer 242 and the second shielding layer 244 can be patterned simultaneously so that they are formed in the gaps between neighboring gate lines 232 or neighboring source lines 234. Hence, compared with other designs having a shielding layer that covers the lead lines completely, resistance-capacitance (RC) delay of the present invention is significantly reduced. Obviously, in the events of errors during the fabrication process, the shielding layer (the first shielding layer 242 and the second shielding layer 244) and the light-leaking region (the gaps between neighboring gate lines 232 and neighboring source lines 234) may partially overlap.

[Para 26] In another embodiment of the present invention, the first shielding layer 242 and the second shielding layer 244 may extend into the first bonding pads 242a and the second bonding pads 244a to reduce light leakage at an angle. Figs. 6 and 7 are top views showing first bonding pads and second bonding pads according to another embodiment of the present invention. In Fig. 6, the first shielding layer 242 extended to cover the gaps between neighboring first bonding pads 232a aside from the gaps between neighboring gate lines 232. In Fig. 7, the second shielding layer 244 extended to cover the gaps between neighboring second bonding pads 234a aside from the gaps between neighboring source lines 234.

[Para 27] Furthermore, one other aspect of the present invention is that a common voltage may be applied to the first shielding layer 242 and the second shielding layer 244. The application of a common voltage reduces signal interference between lead lines (the gate lines 232 or the source lines 234) and thereby reduces the deterioration of pixel quality. Moreover, the voltage also facilitates in the determination of any short circuit between the lead lines and the shielding layer of the thin film transistor array by performing an electrical inspection testing process.

[Para 28] Figs. 8E through 8E are schematic cross-sectional views showing the steps for fabricating a thin film transistor array substrate according to an embodiment of the present invention. As shown in Fig. 8A, a transparent substrate 202 having a pixel region 212a and a peripheral region 212b thereon is provided. The transparent substrate 202 is a glass substrate or a plastic substrate, for example.

[Para 29] As shown in Fig. 8B, a metallic layer (not shown) is formed in the pixel region 212a. The metallic layer is patterned to form a patterned gate layer 214 within the pixel region 212a and a plurality of gate lines 232 and a plurality of first bonding pads (not shown) connected to the gate lines 232 within the peripheral region 212b. The metallic layer is formed in a sputtering operation, for example.

[Para 30] As shown in Fig. 8C, an insulating layer 216 is formed over the transparent substrate 202 to cover the gate layer 214 in the pixel

region 212a and the gate lines 232 in the peripheral region 212b. The insulating layer 216 is a silicon nitride layer or a silicon oxide layer formed, for example, by performing a plasma-enhanced chemical vapor deposition process.

[Para 31] As shown in Fig. 8D, a channel layer (not shown) is formed over the insulating layer 216. The channel layer is patterned to form a channel layer 218 over the insulating layer 216 above the gate 212. The channel layer 218 is fabricated using an amorphous silicon (a-Si) layer, for example.

[Para 32] As shown in Fig. 8E, another metallic layer (not shown) is formed over the transparent substrate 202. The metallic layer is etched to form a patterned source/drain layer 220 within the pixel region 212a, and a plurality of source lines 234 and a plurality of second bonding pads (not shown) connected to the source lines 234 within the peripheral region 212b. Furthermore, a first shielding layer 242 is formed covering the gaps between neighboring gate lines 232. According to one embodiment of the present invention, the first shielding layer 242 may extend into regions over the gaps between neighboring first bonding pads.

[Para 33] Obviously, other protective layers such as a passivation layer 222 (as shown in Fig. 3), an electrode film (not shown) and an orientation film (not shown) may also be fabricated over the substrate 202. Since the processes of fabricating the aforementioned films are well-known to those skilled in the art, detailed description thereof are omitted herein.

[Para 34] In one embodiment of the present invention, a second shielding layer 244 (as shown in Figs. 5 and 7) may be patterned in the process of fabricating the gate layer 214. The second shielding layer 244 is formed underneath the gaps between subsequently formed neighboring source lines 234. According to one embodiment of the invention, the second shielding layer 244 may extend into regions underneath the gaps between subsequently formed neighboring second bonding pads.

[Para 35] In summary, in the thin film transistor array substrate and the fabricating method thereof according to the present invention, a shielding

layer is formed within the peripheral region in locations where light might possibly leak out. The shielding layer formed together with the gate layer is able to reduce any light leakage from the gaps between the source lines and the bonding pads. On the other hand, the shielding layer formed together with the source/drain layer is able to reduce light leakage from the gaps between the gate lines and the bonding pads. Obviously, the shielding layer may be fabricated to cover the gaps between the gate lines or the source lines alone or some other areas within the peripheral region where the probability of light leakage from that location is high. It should be noted that the shielding layer is formed together with the gate layer or the source/drain layer of the thin film transistor in the above embodiments. However, the shielding layer is not limited to be formed together with the gate layer or the source/drain layer. The shielding layer may also be formed not together with the gate layer or the source/drain layer. The shielding layer can be constituted of metal, black resin or other suitable shielding materials.

[Para 36] In conclusion, the thin film transistor array substrate and manufacturing method thereof has at least the following characteristics and advantages:

[Para 37] 1. The shielding layer is patterned to reduce the amount of overlap between the shielding layer and the lead line so that resistance-capacitance delay between the shielding layer and the lead lines is greatly reduced.

[Para 38] 2. The shielding layer may extend into the gaps between bonding pads to reduce light leakage from the substrate at an angle.

[Para 39] 3. A common voltage can be applied to the shielding layer to reduce signal interference between neighboring lead lines and improve display quality.

[Para 40] 4. The application of a common voltage to the shielding layer also facilitate the determination of any short circuit between the lead lines and the shielding layer in a post fabrication electrical inspection of the thin film transistor array.

[Para 41] 5. The shielding layer is formed together with the thin film transistor array so that no need additional process steps are required without impacting the processing time and the production cost.

[Para 42] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.